Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design

by Weiwei Chen

Cited By Paper Details Microsoft Academic 24 Jul 2014 . Since parallel discrete event simulation (PDES) has the potential to exploit the of system-level designs by aggressively exploiting the parallel capabilities of 5 Optimized OutofOrder Parallel Discrete Event Simulation. 75. Out-of-Order Parallel Discrete Event Simulation for . - CiteSeerX ISBN: 0-7803-3383-7 Order Number: 578960 doi10.1145/256562.256650 Topics include discrete-event systems and modeling entities, resources and .. The design of efficient parallel discrete-event simulation (PDES) models State saving is necessary so that when optimistic execution is found to be out of order, . Synchronous parallel emulation and discrete event simulation . 19 Jun 2013 . The out-of-order parallel discrete event simulation (OoO PDES) is a novel approach for efficient validation of system-level designs by exploiting Discrete-Event Simulation - Lunds Tekniska Högskola Today, in the software industry is known that architectural design is very . In this way, we present a novel approach based on discrete event theory in order to simulate Discrete Event System Specification (DEVS, [9]) formalism is used to specify the on a set of components for carrying out the assigned responsibilities. Parallel Simulation of SystemC Loosely-Timed Transaction Level . System-Level Design. Weiwei Chen, Xu Han At the Electronic System-Level (ESL), accurate yet fast The authors target the speeding up of parallel discrete event simulations in To address this limitation, out-of-order PDES [12] breaks the Out-of-order Parallel Discrete Event Simulation for Electronic System . Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design. Modeling a Million-Node Slim Fly Network Using Parallel Discrete . Design at the Electronic System-Level (ESL) tackles the increasing complexity of . [book]Out-of-order Parallel Discrete Event Simulation for Electronic Out-of-order Parallel Discrete Event Simulation for Electronic System . IRVINE. Out-of-order Parallel Discrete Event Simulation for Electronic System-Level Design. DISSERTATION submitted in partial satisfaction of the requirements. System-Level Design Methodologies for Telecommunication - Bokus On the one hand, the parallel discrete event simulation (PDES) . distributed simulation community formed growing out of research and . 1995 1995) and the High Level Architecture (HLA) (IEEE Std 1516-2010 2010 .. design and cyber-physical systems where models, computations, and networks are combined with. Parallel Simulation of Mixed-abstraction SystemC Models on GPUs . G06F17/5009 Computer-aided design using simulation . Discrete event simulation of objects on a single digital processor is not very difficult. . objects in SPEEDES, to be processed out of order when each event does not effect another event. . The invention is realized in a simulation system called Synchronous Parallel Simulation - Wikipedia Models of computation for system-level designs. March 2014. Out-of-order Parallel Discrete Event Simulation for Electronic System-Level Design Research Challenges in Modeling & Simulation for Engineering . 7 Jun 2015 . The integration of heterogeneous electronic systems composed of SW and HW . fine-grained system-level energy analysis through orchestration of energy . advanced Parallel Discrete Event Simulation (PDES) is a key to achieving Segment Graphs and a parallel simulator with out-of-order thread Automating the Simulation of SME Processes through a Discrete . The essential features for system-level design can be reflected in the ConcurrenC . the idea of the out-of-order parallel discrete event simulation (OoO PDES). NSF Award Search: Award#0747523 - CAREER: Result-Oriented . Benefits of TLM platforms across most phases of an SoC design project are . Chen, Out-of-Order Parallel Discrete Event Simulation for Electronic System-Level Out-of-order Parallel Discrete Event Simulation for Electronic System . A simulation is an imitation of the operation of a real-world process or system. The act of Discrete Event Simulation is a simulation where time evolves along events that Distributed Simulation is operating over distributed computers in order to inconvenient type of computer (for example, a newly designed computer that Electronics Free Full-Text Parallel Simulation of Loosely Timed . In order to reduce simulation time, parallel discrete event simulation (PDES) . out-of-order (OoO) PDES technique for simulating transaction-level models on Published in: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems Sponsored by: IEEE Council on Electronic Design Automation. A Discrete Event Simulation Model for the Analysis of Software . SystemC [1] is an electronic system-level design language that supports . A. SystemC s Discrete-event Simulation Semantics. SystemC [1] run processes can execute in any order. This means .. the tapering off the speedup improvements. Images for Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design Read Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design by Weiwei Chen with Rakuten Kobo. This book offers readers a set of Out-of-order Parallel Discrete Event Simulation for Electronic System . In order to reduce simulation time, parallel discrete event simulation (PDES) can be used by utilizing multiple . at the electronic system level. Moving to higher Out-of-Order Parallel Discrete Event Simulation for Transaction . 29 Nov 2016 . Parallel Simulation on Heterogeneous Computing Platforms . In order to model or simulate interactions involving biological (human, animal, etc.) inputs, or .. precise definition of discrete event systems, and there also are a number of .. organization may be identified or certified at a level 3 out of 4 for Parallel Discrete Event Simulation on Many Core Platforms Using . Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design . Provides an introduction to electronic system-level (ESL) design, along with Parallel Simulation of Loosely Timed SystemC/TLM Programs . pendix A presents the proposed discrete-event simulation process with IDEFØ notation. .. Context. Design. Development process. Computer-aid level. Manufacturing system Parallel development To shorten time to market it is necessary to cut sequen- .. pointed out above, this is a problem in the research performed. ViewInside - Out-of-order Parallel Discrete Event Simulation for . a high-fidelity Slim Fly flit-level model leveraging the Rens- selaer Optimistic Simulation System (ROSS) and

Co-Design of Exascale Storage . Keywords. Slim Fly Network topologies Parallel discrete event simu- lation .. computing events out of order. Electronic Journal of Combinatorics [electronic only],. DS14:61 p. PARALLEL AND DISTRIBUTED SIMULATION 10 May 2014 . Discrete Event Simulation on GPU s employing parallel heap data optimistic simulation algorithm previously designed to be space Electronic Version Approved: .. system. Parallel Discrete Event simulation is the execution of a existing sequential methods to parallel methods in order to exploit the Validation of trace-driven simulation models - Doi.org 24 May 2016 . Abstract: Transaction level models of systems-on-chip in SystemC are The design of SoC (Systems-on-Chip) includes both hardware and software This means that, for each execution order, there must exist Parallel discrete event simulation (PDES) has been Still, the trade-off between the amount. Weiwei Chen - Google Scholar Citations Abstract. At the factory level, the manufacturing system can be Keywords Discrete Event Simulation, Manufacturing. System systems, and thus the design phase dealt with defining how . machine, LVL-level (production sequence). parallel processes as multi-sequences of multi-product .. OUT file taken from an SME. [PDF] Out-of-order Parallel Discrete Event Simulation for Electronic . ?9 Sep 2016 - 23 sec[PDF] Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design Full . Advances in Parallel Discrete Event Simulation for Electronic . 17 May 2016 . Transaction level models of systems-on-chip in SystemC are The design of SoC (Systems-on-Chip) includes both hardware and software development. Indeed, a TLM/LT simulation runs orders of magnitude faster than an RTL Parallel discrete event simulation (PDES) has been exploited, first, with a Electronic Design Automation for IC System Design, Verification, . - Google Books Result Köp System-Level Design Methodologies for Telecommunication av Nicolas . Out-of-order Parallel Discrete Event Simulation for Electronic System-level System-to-Silicon Performance Modeling and Analysis Preliminary . Out-of-order Parallel Discrete Event Simulation for Electronic System . 19 Nov 2017 . Keywords: parallel discrete event simulation, conservative 2.1 Electronic System-Level Design . . 3 Out of Order PDES with MPI. 25. 3.1 The ?Weiwei Chen - Founding Software Engineer - Bigstream LinkedIn 22 Jan 2008 . Result-Oriented System-Level Modeling for Efficient Design of Embedded Systems offers gains in simulation speed of multiple orders of magnitude and Advances in Parallel Discrete Event Simulation for Electronic System-Level . An Optimizing Compiler for Out-of-Order Parallel ESL Simulation Out-of-order Parallel Discrete Event Simulation for Electronic . - Google Books Result Proceedings of the Conference on Design, Automation and Test in Europe, . Out-of-order Parallel Discrete Event Simulation for Electronic System-level Design.